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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

**Tohru WATANABE**

Serial No: Not yet assigned

Filed: March 17, 2000

For: **SOLID-STATE IMAGE PICKUP APPARATUS**JCS25 U.S. PTO  
09/531135  
03/17/00

Box PATENT APPLICATION

Assistant Commissioner for Patents

Washington, D.C. 20231

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Transmitted herewith for filing is the patent application identified above.

- ☒ 6 sheets of drawings (☒ formal ☐ informal) are enclosed.
- ☒ 27 pages of specification and 1 page of abstract of the invention are enclosed.
- ☒ An assignment of the invention to Sanyo Electric Co., Ltd. ☒ is enclosed ☐ will follow.
- ☐ An associate power of attorney ☐ is enclosed ☐ will follow.
- ☐ A verified statement to establish small entity status under 37 C.F.R. §§ 1.9 & 1.27 is enclosed.
- ☒ Declaration and Power of Attorney ☐ is enclosed ☐ will follow.
- ☒ A certified copy of Japanese Patent Application No. Hei 11-073930 filed March 18, 1999 from which priority is claimed under 35 U.S.C. § 119 is enclosed.
- ☐ IDS enclosed (☐ with references).
- ☐ Preliminary Amendment is enclosed.

## CALCULATION OF FEES

ITEM	TOTAL NO. OF CLAIMS		NO. OF CLAIMS OVER BASE	LG/SM \$ ENTITY FEE	\$ AMOUNT	\$ FEE
A TOTAL CLAIMS FEE	10	-20	0	LG=\$18 SM=\$9	\$	\$ 0
B INDEPENDENT CLAIMS FEE*	3	-3	0	LG=\$78 SM=\$39	\$	\$ 0
C SUBTOTAL - ADDITIONAL CLAIMS FEE (ADD FINAL COLUMN IN LINES A + B)						\$ 0
D MULTIPLE-DEPENDENT CLAIMS FEE				LARGE ENTITY FEE = \$260 SMALL ENTITY FEE = \$130		\$
E BASIC FEE				LARGE ENTITY FEE = \$690 SMALL ENTITY FEE = \$345		\$ 690
F TOTAL FILING FEE (ADD TOTALS FOR LINES C, D, AND E)						\$ 690
G ASSIGNMENT RECORDING FEE					\$ 40	\$ 40
*LIST INDEPENDENT CLAIMS 1, 4 and 7						

"Continued on Second Page"

- ☒ A check in the amount of \$ 690 to cover the filing fee is enclosed.
- ☒ A check in the amount of \$ 40 to cover Assignment Recordation fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge any deficiency for the following fees associated with this communication or credit any overpayment to Deposit Account No. 12-1820. **A copy of this sheet is enclosed.**
- ☒ Any additional filing fees required under 37 C.F.R. § 1.16
- ☒ Any patent application processing fees under 37 C.F.R. § 1.17
- Please associate this application with the attorneys of record and with the correspondence address recorded for Customer No. 22335.

Respectfully submitted,  
LOEB & LOEB LLP

By: 

WILLIAM H. WRIGHT  
Registration No. 36,312  
Attorney for Applicant

Date: 17 March 2000

10100 Santa Monica Blvd., 22nd Floor  
Los Angeles, California 90067-4164  
Telephone: 310-282-2260  
Facsimile: 310-282-2192

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jc712 U.S. PTO

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Tohru WATANABE

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Dear Sir:

I hereby certify that

- ☒ two copies of a letter of transmittal
- ☒ check in amount of \$ 690.00 as filing fee
- ☒ patent application ( 27 pages of specification; 10 claims; 1 page of abstract
- ☒ 6 sheets of formal drawings
- ☒ executed Declaration and Power of Attorney
- ☒ assignment of the invention to Sanyo Electric Co., Ltd.
- ☒ certified copy of Japanese patent application No. Hei 11-073930 which was filed March 18, 1999 from which priority is claimed in the subject case pursuant to 35 U.S.C. § 119
- ☐ Preliminary Amendment
- ☒ Information Disclosure Statement with      references
- ☐ return postcard

are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service with sufficient postage under 37 C.F.R. § 1.10 on the date indicated above and are addressed to:

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Date: 17 March 2000

10100 Santa Monica Blvd., 22nd Floor  
Los Angeles, California 90067-4164  
Telephone: 310-282-2260  
Facsimile: 310-282-2192

Sherry J. Batalla

Name of person mailing papers

Signature

# SOLID-STATE IMAGE PICKUP APPARATUS

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

5 The present invention relates to a solid-state image pickup apparatus configured using a solid-state image pickup device of the frame transfer system.

### 2. Description of the Prior Art(s)

10 Fig. 1 is a top plan view schematically showing a CCD solid-state image pickup device of the frame transfer system, and Fig. 2 is a timing chart illustrating the operation of the solid-state image pickup device.

15 The solid-state image pickup device of the frame transfer system comprises a light receiving section 1, a storage section 2, a horizontal transfer section 3, and an output section 4. The light receiving section 1 comprises a plurality of shift registers, having a plurality of consecutive bits in the vertical direction, arranged so as to be parallel to each other. Each bit of these shift registers forms a light receiving bit. Each light receiving bit generates and accumulates an information charge corresponding to an object image. The storage section 2 is formed from a plurality of shift registers consecutive to each shift register of the light receiving section 1. Each bit of these shift registers forms a storage bit, and each storage bit temporarily stores the information charge transferred from the light receiving section 1. The horizontal transfer section 3

20

25

comprises a single shift register, to which each bit is connected the respective output of the plurality of shift registers of the storage section 2, and receives, then sequentially transfers and outputs in the horizontal direction, one line at a time the information charges of one screen stored in the storage section 2. The output section 4 is formed from an electrically independent capacitor and an amplifier obtaining the change in electric potential of the capacitor, and the information charge that is output from the horizontal transfer section 3 is received at the capacitor one bit at a time and converted to a voltage value and output as image signal Y0.

To the light receiving section 1 is applied a frame transfer clock  $\phi F$  for transferring at high speed the information charge of the light receiving section 1 to the storage section 2 within the blanking period of a vertical scan in synchronization with a vertical synchronization signal VD. To the storage section 2 is applied a vertical transfer clock  $\phi V$  for loading the information charges that are transferred and output from the light receiving section 1 by the frame transfer clock  $\phi F$  as well as for transferring the loaded information charges for one screen to the horizontal transfer section 3 one line at a time within the blanking period of a horizontal scan in synchronization with a horizontal synchronization signal HD. Then, to the horizontal transfer section 3 is applied a horizontal transfer clock  $\phi H$  for transferring the information charges that are loaded into

the horizontal transfer section 3 one line at a time in response to the vertical transfer clock  $\phi_V$  to the sequential output section 4 in synchronization with the horizontal synchronization signal HD. As a result, the information charges generated at the light receiving section 1, after being transferred to the storage section 2 in one-screen units, are transferred and output one line at a time to the output section 4 via the horizontal transfer section 3, and the image signal Y0 is output in consecutive one-line units.

Furthermore, a substrate clock  $\phi_B$ , which rises for a predetermined period during the vertical scan period, is applied to the semiconductor substrate that forms the solid-state image pickup device. In response to the rise of the substrate clock  $\phi_B$ , the frame transfer clock  $\phi_F$  is clocked at the same period as during frame transfer, and the information charges of the light receiving section 1 are completely discharged to the substrate. Therefore, a period L, from the completion of the discharge operation of information charges by the substrate clock  $\phi_B$  to the initiation of the transfer operation by the frame transfer clock  $\phi_F$ , becomes the storage time of the information charges. The image signal Y0 represents a level that is proportional to the quantity of information charges stored in each light receiving pixel of the light receiving section 1 during the storage time L.

In the case of the solid-state image pickup device of the frame transfer system, the storage performance of the information charge of each light receiving pixel is attributed

to the capacity of the potential well formed within the substrate by action of the transfer electrode located in the light receiving section 1. The capacity of this potential well is determined, for example, by the width of the transfer electrode and width of the transfer channel, and further the voltage of the pulse driving the transfer electrode.

When the width of the transfer electrode or width of the transfer channel narrows with the increased resolution of the solid-state image pickup device, the capacity of the potential well that is formed decreases and the storage performance of the information charge of each light receiving pixel lowers. Furthermore, when the driving pulse is lowered in voltage in order to reduce the power consumption of the device, the capacity of the potential well that is formed decreases further. Therefore, the dynamic range of the solid-state image pickup device becomes narrow and the image pickup conditions become restricted.

#### SUMMARY OF THE INVENTION

It is therefore an object of the present invention to extend the dynamic range of the solid-state image pickup device and perform image pickup operations over a wide range.

The present invention comprises a solid-state image pickup device in which a first light receiving pixel is arranged in a plurality of lines in one line units and a second light receiving pixel capable of being driven independently from the first light receiving pixel is arranged

in at least one line units between first light receiving  
pixels of the plurality of lines, a drive circuit for driving  
the first and second light receiving pixels of the solid-state  
image pickup device and performing accumulation of the  
5 information charges at mutually different times between the  
first light receiving pixel and second light receiving pixel  
as well as transferring and outputting the information charges  
accumulated in the first and second light receiving pixels  
independently of each other, a timing control circuit for  
10 respectively setting the storage time of information charges  
at the first light receiving pixel and the storage time of  
information charges at the second light receiving pixel of the  
solid-state image pickup device, and a signal processing  
circuit for generating an image signal by adding a first  
15 output corresponding to the first light receiving pixel and a  
second output corresponding to the second light receiving  
pixel of the solid-state image pickup device.

According to the present invention, image signals are  
generated by adding together the outputs corresponding to two  
20 types of light receiving pixels for which the accumulation  
time of information charges can be set independently.  
Therefore, for an object of low brightness, a sufficient  
output can be obtained from a light receiving pixel for which  
a long accumulation time of information charges has been set,  
25 and for an object of high brightness, a wide range of image  
pickup is possible from a light receiving pixel for which a  
short accumulation time of information charges has been set.



## BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic top plan view of a solid-state image pickup device of a frame transfer system.

Fig. 2 is a timing chart illustrating the operation of the solid-state image pickup device of the frame transfer system.

Fig. 3 is a block diagram showing a configuration of the solid-state image pickup device of the present invention.

Fig. 4 is a timing chart illustrating the operation of the solid-state image pickup device of the present invention.

Fig. 5 is a waveform diagram of the image data in an analog representation.

Fig. 6 is a potential diagram showing one example of the operation of the solid-state image pickup device of the present invention.

Fig. 7 is a waveform diagram of the transfer clocks achieving the operation of Fig. 6.

Fig. 8 shows a relationship between quantity of received light and output voltage.

Fig. 9 shows a relationship between signal component and smear component.

Fig. 10 is a potential diagram showing another example of the operation of the solid-state image pickup device of the present invention.

Fig. 11 is a waveform diagram of the transfer clocks achieving the operation of Fig. 10.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 3 is a block diagram showing the configuration of the solid-state image pickup device of the present invention and Fig. 4 is a timing chart illustrating the operation thereof.

A solid-state image pickup device 11 is identical to the solid-state image pickup device of the frame transfer system shown in Fig. 1, and comprises the light receiving section 1, the storage section 2, the horizontal transfer section 3, and the output section 4. A drive circuit 12 generates in response to various timing signals and supplies to the solid-state image pickup device 11 the frame transfer clock  $\phi F$ , the vertical transfer clock  $\phi V$ , the horizontal transfer clock  $\phi H$ , and the substrate clock  $\phi B$ . The frame transfer clock  $\phi F$  is applied to the light receiving section 1, and the transfer electrode is clocked at a timing in accordance to the rise of the substrate clock  $\phi B$  and the information charges of the light receiving section 1 are transferred at high speed to the storage section 2 within the blanking period of the vertical scan in synchronization with the vertical synchronization signal VD. The substrate clock  $\phi B$  is applied to the semiconductor substrate forming the solid-state image pickup device, is made high for a predetermined period at a timing in accordance to a shutter timing signal ST, and causes the information charges of the light receiving section 1 to be discharged to the substrate by action of the frame transfer clock  $\phi F$ . Therefore, to each light receiving pixel of the

light receiving section 1 are accumulated the information charges during the period L, from completion of the discharge operation by the substrate clock  $\phi B$  to initiation of the transfer operation by the frame transfer clock  $\phi F$ .

5       The solid-state image pickup device 11 has an arrangement in the vertical direction of pixels, the number of which is at least twice the required number of scanning lines. Namely, a plurality of light receiving pixels arranged vertically corresponds to one scanning line. These light receiving  
10 pixels can be set so that the accumulation times of the information charges are mutually different, and for these light receiving pixels, at least two types of accumulation times are set. Accordingly, the shutter timing signal ST sets the timing of the shutter operation into multiple steps. The  
15 shutter operation in the present embodiment refers to the discharging of the information charges accumulated in a pixel and the transferring of the information charges of a particular pixel to another pixel. For example, pixels are arranged in the vertical direction, the number of which is  
20 twice the number of scanning lines for displaying the reproduction screen, and the accumulation times of the information charges are set independently for the odd-numbered lines and for the even-numbered lines. The following operation is given for the case where the light receiving  
25 pixels, the number of which is twice the number of the horizontal scanning lines, are arranged in the vertical direction, and the accumulation times for the information

charges are set with a difference between the light receiving pixels of the odd-numbered lines and the light receiving pixels of the even-numbered lines.

The vertical transfer clock  $\phi V$  is applied to the storage  
5 section 2, the information charges transferred and output from the light receiving section 1 by the frame transfer clock  $\phi F$  are loaded to the storage section 2, and the loaded information charges for one screen are transferred one line at a time to the horizontal transfer section 3 at one half the  
10 period of the horizontal synchronization signal HD. The horizontal transfer clock  $\phi H$  is then applied to the horizontal transfer section 3, the information charges loaded into the horizontal transfer section 3 are sequentially transferred to the output section 4 at every line in synchronization with the  
15 vertical transfer clock  $\phi V$ . As a result, the information charges accumulated at each light receiving pixel of the light receiving section 1 during the period L are transferred to the storage section 2 in one-screen units, then transferred and output one line at a time to the output section 4 via the  
20 horizontal transfer section 3, and the image signal Y0 is output in consecutive in one-line units.

A timing control circuit 13 generates and supplies to the drive circuit 12 the horizontal synchronization signal HD and vertical synchronization signal VD on the basis of a reference  
25 clock having a fixed period. Furthermore, the shutter timing signal ST, which rises during the vertical scan, is generated and supplied to the drive circuit 12. The shutter timing

signal ST is a 2-bit signal, for example, and sets the timing of the shutter operation in two steps. A ratio R of the substantial accumulation times of the information charges generated from the delay in shutter operation is supplied to the arithmetic circuit 20 to be described hereinafter. At this time, a value  $1/(R-1)$  is generated in correspondence to ratio R of the accumulation times and simultaneously supplied to the arithmetic circuit 20.

An analog processing circuit 14 executes a sample and hold operation and various types of correction operations for the image signal Y0 that is input from the solid-state image pickup device 11 and generates an image signal Y1 conforming to a predetermined format. For example, to generate the image signal Y1, the sample and hold operation is performed at the timing for obtaining only the signal level for the image signal Y0 in which the reset level and signal level repeat in synchronization with the output operation of the solid-state image pickup device 11. An A/D converter circuit 15 synchronizes with the sample and hold operation of the analog processing circuit 14 and generates image data D1 representing information on each light receiving pixel of the solid-state image pickup device 11. At the solid-state image pickup device 11, in the case where the accumulation time of the information charges differs between the light receiving pixel of the odd-numbered lines and the light receiving pixel of the even-numbered lines, the image data D1 is obtained for two lines during the horizontal scan period as shown in Fig. 5.

At this time, the level of the image data D1 for two lines obtained within the same horizontal scan period contains a difference proportional to the ratio of the accumulation times of the information charges in each light receiving pixel of the solid-state image pickup device 11.

A line memory 16 stores the image data D1 for one line during the first half of each horizontal scan period. The image data D1 stored in the line memory 16 is read out as the image data D2 after a delayed timing of half the horizontal scan period. The line memory 16 is configured, for example, by arranging in parallel two memory circuits, each having the capacity for storing one line of image data D1, so as to alternately perform read and write operations of the image data D1.

The arithmetic circuit 20, comprising first and second multipliers 21 and 22, first through third subtracters 23, 24, and 25, and an adder 26, operates during the period when a gate pulse GP rises and generates a smear data S and a third image data D3. The first multiplier 21 multiplies the ratio R that is input from the timing control circuit 13 with the first image data D1, and the first subtracter 23 subtracts the second image data D2 from the multiplication result  $R \cdot D1$  of the first multiplier 21. The second multiplier 22 multiplies  $1/(R-1)$  that is input from the timing control circuit 13 with the subtraction result S0 of the first subtracter 23. The multiplication result of the second multiplier 22 is output as smear data. The second subtracter 24 subtracts the smear data

S from the second data D2, and the third subtracter 25 subtracts the smear data S from the first data D1. The adder 26 then adds the subtraction result D2' of the second subtracter 24 and the subtraction result D1' of the third subtracter 25, and outputs the addition result as the third image data D3.

Fig. 6 is a potential diagram showing one example of a method for driving the solid-state image pickup device in the solid-state image pickup apparatus of the present invention, and Fig. 7 is a timing chart of the transfer clocks achieving the operation thereof. These figures illustrate the case where the light receiving pixels, the number of which is twice the number of scanning lines, are arranged in the vertical direction in the light receiving section 1 of the solid-state image pickup device 11, and the accumulation times of the information charges are set with a difference between the light receiving pixels of the odd-numbered lines and the light receiving pixels of the even-numbered lines.

In the light receiving section 1 of the solid-state image pickup device 11, a plurality of transfer electrodes are arranged in correspondence to six phases of transfer clocks  $\phi 1$  through  $\phi 6$ , and with respect to the transfer electrodes of the six phases, two pixels P1 and P2 are substantially defined.

At the initiation of the first image pickup operation, the second transfer clock  $\phi 2$  and the fifth transfer clock  $\phi 5$  rise, and the potential levels under the respective transfer electrodes applied with the transfer clocks  $\phi 2$  and  $\phi 5$  are

deeply formed. At this time, the other transfer clocks  $\phi_1$ ,  $\phi_3$ ,  $\phi_4$ , and  $\phi_6$  remain low, and the potential levels under the transfer electrodes applied with the transfer clocks  $\phi_1$ ,  $\phi_3$ ,  $\phi_4$ , and  $\phi_6$  remain shallow. As a result, at a timing  $t_0$  during the first charge accumulation period, potential wells are formed under the transfer electrodes applied with the transfer clocks  $\phi_2$  and  $\phi_5$ , and at these potential wells are accumulated the information charges generated by photoelectric conversion.

At the elapse of a predetermined period  $L_1$  from the initiation of storage of the information charges, the third transfer clock  $\phi_3$  rises, and in succession, the second transfer clock  $\phi_2$  falls. At a timing  $t_1$  after the second transfer clock  $\phi_2$  falls, the potential well storing information charges, along with the information charges accumulated in period  $L_1$ , moves from under the transfer electrode applied with the second transfer clock  $\phi_2$  to under the transfer electrode applied with the third transfer clock  $\phi_3$ . Furthermore, when the third transfer clock  $\phi_3$  falls after the fourth transfer clock  $\phi_4$  rises, the potential well, along with the information charges, moves from under the transfer electrode applied with the third transfer clock  $\phi_3$  to under the transfer electrode applied with the fourth transfer clock  $\phi_4$ . At this time, the information charges accumulated in period  $L_1$  under the transfer electrode applied with the second transfer clock  $\phi_2$  are combined with the information charges accumulated in the same period  $L_1$  under the transfer electrode applied with the fifth transfer clock  $\phi_5$ .



Then, after the second transfer clock  $\phi_2$  is raised, the fourth transfer clock  $\phi_4$  is lowered and the second image pickup operation is initiated. As a result, at a timing  $t_2$  during the charge accumulation period, similar to the case for timing  $t_0$ , potential wells are formed under the transfer electrodes applied with the transfer clocks  $\phi_2$  and  $\phi_5$ , and at these potential wells are again accumulated the information charges generated by photoelectric conversion. The second image pickup operation continues during period L2.

At the potential well under the transfer electrode applied with the second transfer clock  $\phi_2$ , information charges are hardly stored at the initiation of the second image pickup operation. As a result of this, at the potential well under the transfer electrode applied with the second transfer clock  $\phi_2$ , namely, the first light receiving pixel P1, are stored only the information charges generated during period L2, when the second storage operation is performed. On the other hand, at the potential well under the transfer electrode applied with the fifth transfer clock  $\phi_5$  are stored the information charges accumulated in two potential wells in period L1, when the first image pickup operation was performed. As a result of this, at the potential well under the transfer electrode applied with the fifth transfer clock  $\phi_5$ , namely, the second light receiving pixel P2, the information charges generated during period L3 continuing from the first image pickup operation to the second image pickup operation are accumulated, and furthermore, the information charges

generated at the first light receiving pixel P1 during period L1, when the first image pickup operation is performed, are added.

After completion of the above-mentioned first and second image pickup operations, the first through sixth transfer clocks  $\phi 1$  through  $\phi 6$  are clocked with a mutual phase difference of  $2\pi/3$ , and the information charges of the light receiving pixels P1 and P2 are transferred and output while respectively independent. As a result, the output corresponding to the first light receiving pixel P1 and the output corresponding to the second light receiving pixel P2, namely, the levels of image data D1 and D2 processed in the arithmetic circuit 20 show the following relationship in the period when the gate pulse rises:

$$D1:D2 = L2:(L1+L3)$$

Since the light receiving pixels P1 and P2 usually have equal storage capacities of information charges, the second light receiving pixel P2 becomes saturated at a small quantity of incident light. For example, as shown in Fig. 8, when the output voltage of the first light receiving pixel P1 reaches the saturation level Vs at a quantity of received light m1, the output voltage of the second light receiving pixel P2 reaches the saturation level Vs at a quantity of received light m2, which is smaller than the quantity of received light m1.

In the above-mentioned arithmetic circuit 20, the following processing is executed for the two types of image

data D1 and D2. It is assumed here that the period L1 for performing the first image pickup operation and the period L2 for performing the second image pickup operation are equal, and the period required for transferring the information charge from the first light receiving pixel P1 to the second light receiving pixel P2 is sufficiently smaller than periods L1 and L2 and can thus be ignored. At this time, the ratio R that is input from the timing control circuit 13 is "3" and  $1/(R-1)$  is "1/2".

First, the image data D1 is tripled at the first multiplier 21, and as shown in Fig. 9, the tripled image data 3D1 with a level matching that of the image data D2 is generated. Usually, each image data D1 and D2 contains the proper signal component and the smear component combined by the vertical transfer of information charges so that when the image data D1 is tripled, the smear component besides the signal component is also tripled. Accordingly, at the first subtracter 23, when the image data D2 is subtracted from the tripled image data 3D1, the signal component is canceled out leaving the smear component, thus generating the smear data S0. The smear data S0, which is the result of subtracting the singled smear component from the tripled smear component, actually represents a doubled value. Next, when the smear data S0 is multiplied by 1/2 at the second multiplier 22, the smear data S representing the actual smear component is generated.

At the second and third subtracters 24 and 25, the smear

data S is respectively subtracted from the image data D1 and D2, and image data D1' and D2', which become only the signal components, are generated. The image data D1' and D2' are added together at the adder 26 where a third image data D3 is output.

The aforementioned third image data D3 is obtained by combining the two types of image data D1 and D2 having different light receiving sensitivities, and this substantially extends the dynamic range of the solid-state image pickup device. For example, as shown in Fig. 8, it is possible to vary the output voltage according to the quantity of received light until the quantity of received light reaches  $m_1$ . If only the dynamic range is observed here, the first image data D1 varies over the same range. However, since the first image data D1 drops in light receiving sensitivity at low brightness, a sufficient output cannot be obtained when the quantity of received light is low. In the case of the third image data D3, the dynamic range can be extended while an output of sufficient level is obtained even at low brightness.

Furthermore, the third image data D3 has a different output voltage level with respect to the quantity of received light, namely, a different apparent light receiving sensitivity, when the quantity of received light is between 0 and  $m_2$ , and when the quantity of received light is between  $m_2$  and  $m_1$ . However, from the fact that high sensitivity results when the quantity of received light is low and low sensitivity

results when the quantity of received light is high, any visual deficiency in the reproduction screen can be eliminated if the ratio of periods L1 and L2, when the respective image pickup operations are performed, is optimized and the characteristics of the change in the output voltage with respect to the quantity of received light is approximated to the gamma correction curve.

Furthermore, since the smear data S is calculated at every line, the difference in the smear component in every line generated due to the difference in the transfer distance is correctly represented. Furthermore, since the timing at which this smear component is obtained is nearly identical to the timing at which the smear component is combined into the actual respective image signals of the odd-numbered lines and even-numbered lines, the influence of deterioration with time of the object is minimal.

Fig. 10 is a potential diagram showing another example of a method for driving the solid-state image pickup device in the solid-state image pickup apparatus of the present invention, and Fig. 11 is a timing chart of the transfer clocks achieving the operation thereof. These figures, similar to Fig. 6 and Fig. 7, show the case where the light receiving pixels, the number of which is twice the number of scanning lines, are arranged in the vertical direction in the light receiving section 1 of the solid-state image pickup device 11, and the storage times of information charges are different between the light receiving pixels of the odd-

numbered lines and the light receiving pixels of the even-numbered lines.

When the first image pickup operation is initiated, the fifth transfer clock  $\phi 5$  rises, and the potential level under the transfer electrodes applied with the transfer clock  $\phi 5$  is deeply formed. At this time, the other transfer clocks  $\phi 1$  through  $\phi 4$  and  $\phi 6$  remain low, and the potential levels under the transfer electrodes applied with the transfer clocks  $\phi 1$  through  $\phi 4$  and  $\phi 6$  remain shallow. As a result, at timing  $t_0$  during the first charge accumulation period, a potential well is formed under the transfer electrode applied with the fifth transfer clock  $\phi 5$ , and at this potential well are accumulated the information charges generated by photoelectric conversion.

The first image pickup operation completes at the elapse of period  $L_1$  from the initiation of accumulation of the information charges, and the second image pickup operation is initiated at the rise of the second transfer clock  $\phi 2$ . At the initiation of the second image pickup operation, only the second transfer clock  $\phi 2$  rises, and the other transfer clocks  $\phi 1$  and  $\phi 3$  through  $\phi 6$  remain the same as at the first image pickup operation. At timing  $t_1$  after the initiation of the second image pickup operation, a potential well storing the information charges is also formed under the transfer electrode applied with the second transfer clock  $\phi 2$ . As a result, at timing  $t_2$  during the charge storage period, a potential wells are formed under the respective transfer electrodes applied with the transfer clocks  $\phi 2$  and  $\phi 5$ , and at

these potential wells are again accumulated the information charges generated by photoelectric conversion. The second image pickup operation continues during the period L2.

At the potential well under the transfer electrode applied with the second transfer clock  $\phi_2$ , namely, the first light receiving pixel P1, are accumulated only the information charges generated during the period L2, when the second storage operation is performed. On the other hand, at the potential well under the transfer electrode applied with the fifth transfer clock  $\phi_5$ , namely, the second light receiving pixel P2, are accumulated the information charges generated through the period L1, when the first image pickup operation is performed, and the period L2, when the second image pickup operation is performed.

After the completion of the above-mentioned first and second image pickup operations, similar to the first embodiment, the first through sixth transfer clocks  $\phi_1$  through  $\phi_6$  are clocked with a mutual phase difference of  $2\pi/3$ , and the information charges of the light receiving pixels P1 and P2 are transferred and output while respectively independent. As a result, the output corresponding to the first light receiving pixel P1 and the output corresponding to the second light receiving pixel P2 show the following relationship:

$$P1:P2 = L2:(L1+L2)$$

The image signals obtained in the above-mentioned manner, except for the fact that the ratio of the image signal level corresponding to the first light receiving pixel P1 to the

image signal level corresponding to the second light receiving pixel P2 is different, can be handled in the same manner as the first embodiment. Therefore, expansion of the dynamic range of the solid-state image pickup device and detection of  
5 the smear component become possible.

It should be noted that while examples were given for the case where all lines of the light receiving pixels arranged in the light receiving section were assigned to the first and second light receiving pixels P1 and P2, two adjacent lines  
10 among light receiving pixels arranged with three or more consecutive lines may be assigned to the first and second light receiving pixels P1 and P2. For example, with four lines of light receiving pixels, the first light receiving pixel P1 is assigned to the first line, the second light  
15 receiving pixel P2 is assigned to the second line, and the third and fourth lines perform the storage of information charges individually without performing the combination of information charges from the other pixels.

Furthermore, the line memory 16 and the arithmetic  
20 circuit 20 may respectively comprise a memory circuit capable of storing image data D1 for a suitable number of lines, and a digital signal processing circuit for repeating the reading and writing of data to the memory circuit along with arithmetic operations.

25 According to the present invention, two types of image signals can be obtained from one solid-state image pickup device, and by executing arithmetic operations for these image



signals, expansion of the dynamic range and detection of the smear component become possible.

While there has been described what are at present considered to be preferred embodiments of the invention, it  
5 will be understood that various modifications may be made thereto, and it is intended that the appended claims cover all such modifications as fall within the true spirit and scope of the invention.

WHAT IS CLAIMED IS:

1. A solid-state image pickup apparatus comprising:

a solid-state image pickup device in which a first light  
5 receiving pixel is disposed in a plurality of lines in one-  
line units, and a second light receiving pixel capable of  
being driven independently from said first light receiving  
pixel is disposed in at least one-line units between first  
light receiving pixels of the plurality of lines;

10 a drive circuit for driving the first and second light  
receiving pixels of said solid-state image pickup device and  
accumulating information charges at mutually different times  
between first light receiving pixel and second light receiving  
pixel, as well as transferring and outputting information  
15 charges accumulated in said first and second light receiving  
pixels independently of each other;

a timing control circuit for respectively setting the  
storage time of information charges at the first light  
receiving pixel and the storage time of information charges at  
20 the second light receiving pixel of said solid-state image  
pickup device; and

a signal processing circuit for generating an image  
signal by adding a first output corresponding to the first  
light receiving pixel and a second output corresponding to the  
25 second light receiving pixel of said solid-state image pickup  
device.

2. The solid-state image pickup apparatus according to claim  
1 wherein said signal processing circuit calculates vertical  
transfer smear component on the basis of a ratio of said  
respective accumulation times of information charges at said  
5 first and second light receiving pixels of said solid-state  
image pickup device and of a difference of said first and  
second outputs corresponding to said first and second light  
receiving pixels of said solid-state image pickup device.

10 3. The solid-state image pickup apparatus according to claim  
2 wherein said signal processing circuit subtracts said  
vertical transfer smear component from said image signal on  
the basis of a ratio of said respective accumulation times of  
information charges at said first and second light receiving  
15 pixels of said solid-state image pickup device and of a  
difference of said first and second outputs corresponding to  
said first and second light receiving pixels of said solid-  
state image pickup device.

20 4. The solid-state image pickup apparatus comprising:  
the solid-state image pickup device having a line of  
first light receiving pixels and a line of second light  
receiving pixels disposed so as to respectively correspond to  
horizontal scanning lines and capable of driving independently  
25 of each other said first light receiving pixels and said  
second light receiving pixels;

the drive circuit for driving said first and second light

receiving pixels so that accumulation of information charges is performed at different times between said first light receiving pixels and said second light receiving pixels, as well as transferring and outputting independently of each other said information charges accumulated in said first and second light receiving pixels and generating the first output according to said information charges accumulated in said first light receiving pixels and the second output according to said information charges accumulated in said second light receiving pixels; and

the signal processing circuit for performing calculation of a smear quantity generated during vertical transfer of said information charges at said solid-state image pickup device on the basis of a ratio of said respective accumulation times of said information charges at said first and second light receiving pixels and of said first output and said second output.

5. The solid-state image pickup apparatus according to claim 4 wherein said signal processing circuit performs calculation of said smear quantity for every pair of said first light receiving pixel and said second light receiving pixel disposed so as to be in mutual proximity on same vertical transfer path.

6. The solid-state image pickup apparatus according to claim 4 wherein said signal processing circuit removes smear

component included in at least said first output or said second output on the basis of said smear quantity of said calculation.

5 7. The solid-state image pickup apparatus comprising:

the solid-state image pickup device having a line of first light receiving pixels and a line of second light receiving pixels disposed so as to respectively correspond to horizontal scanning lines and capable of driving independently of each other said first light receiving pixels and said second light receiving pixels;

10 the drive circuit for driving said first and second light receiving pixels so that accumulation of information charges is performed at different times between said first light receiving pixels and said second light receiving pixels, as well as transferring and outputting independently of each other said information charges accumulated in said first and second light receiving pixels and generating the first output according to said information charges accumulated in said first light receiving pixels and the second output according to said information charges accumulated in said second light receiving pixels; and

15 the signal processing circuit for generating an image signal by adding together said first output and said second output corresponding to identical horizontal scanning lines.

8. The solid-state image pickup apparatus according to claim

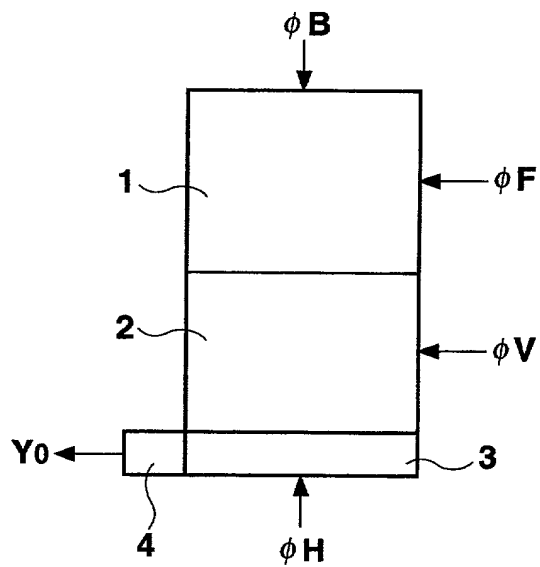
7 wherein said signal processing circuit performs calculation  
of smear quantity generated during vertical transfer of said  
information charges at said solid-state image pickup device on  
the basis of a ratio of said respective accumulation times of  
5 said information charges at said first and second light  
receiving pixels and of said first output and said second  
output.

9. The solid-state image pickup apparatus according to claim  
10 8 wherein said signal processing circuit performs calculation  
of said smear quantity for every pair of said first light  
receiving pixel and said second light receiving pixel disposed  
so as to be in mutual proximity on same vertical transfer  
path.

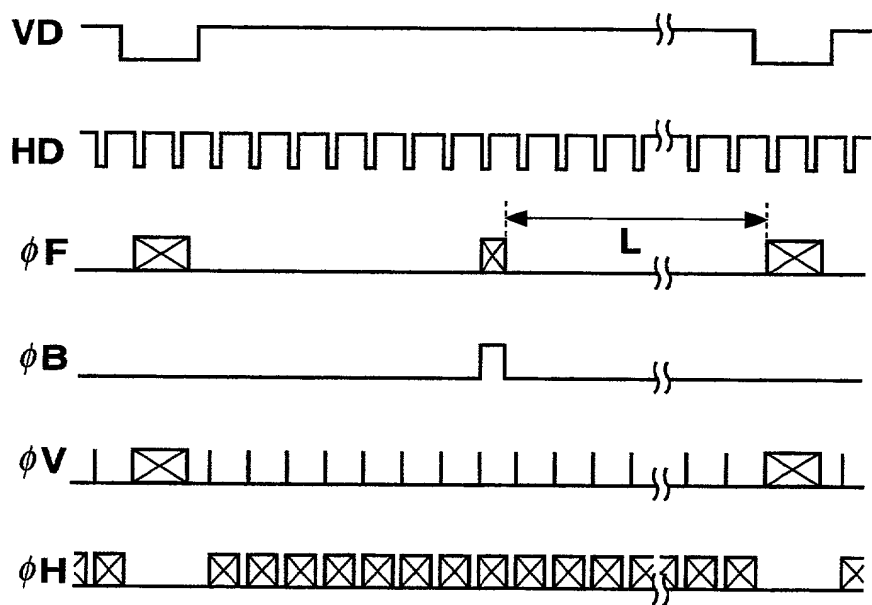
15 10. The solid-state image pickup apparatus according to claim  
8 wherein said signal processing circuit removes smear  
component included in said image signal on the basis of said  
smear quantity of said calculation.

## ABSTRACT OF THE DISCLOSURE

Two types of image signals are obtained from a solid-state image pickup device in a frame transfer system and  
5 subject to signal processing so as to extend the dynamic range. Two types of mutually different image signals are obtained from a solid-state image pickup device (11). The two types of image signals obtained through time division are matched in timing by a line memory (16). An arithmetic  
10 circuit (20) multiplies image data D1 with ratio R of storage times and subtracts image data D2 from the multiplication result  $R \cdot D1$  so as to generate smear data S0. The smear data S0 is multiplied with  $1/(R-1)$  so as to generate smear data S representing the proper smear component. The smear data S is  
15 subtracted from image data D1 and D2, and the subtraction results are added to generate image data D3.

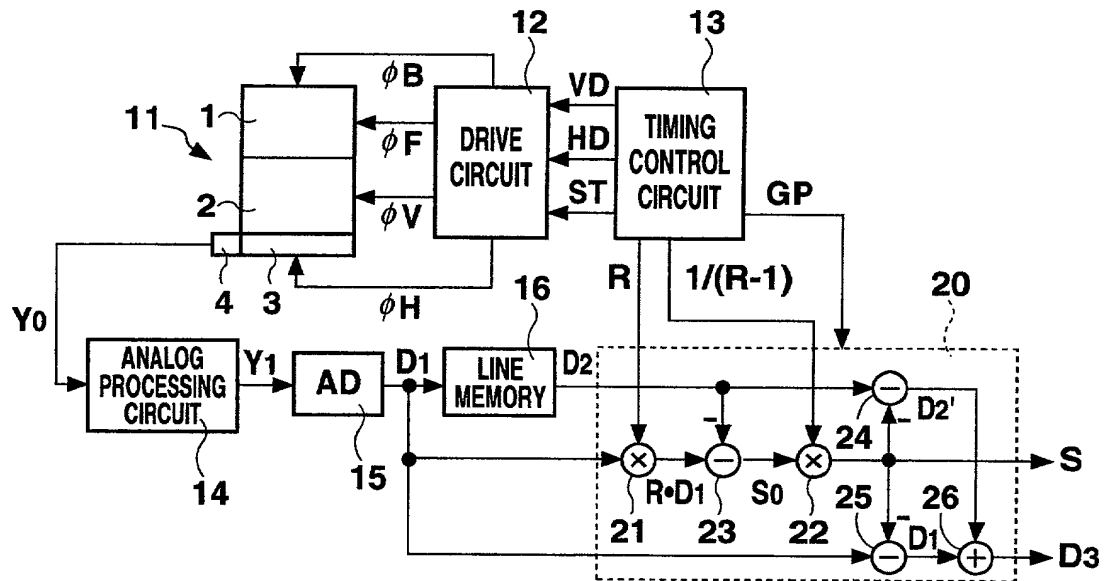


**Fig. 1 RELATED ART**

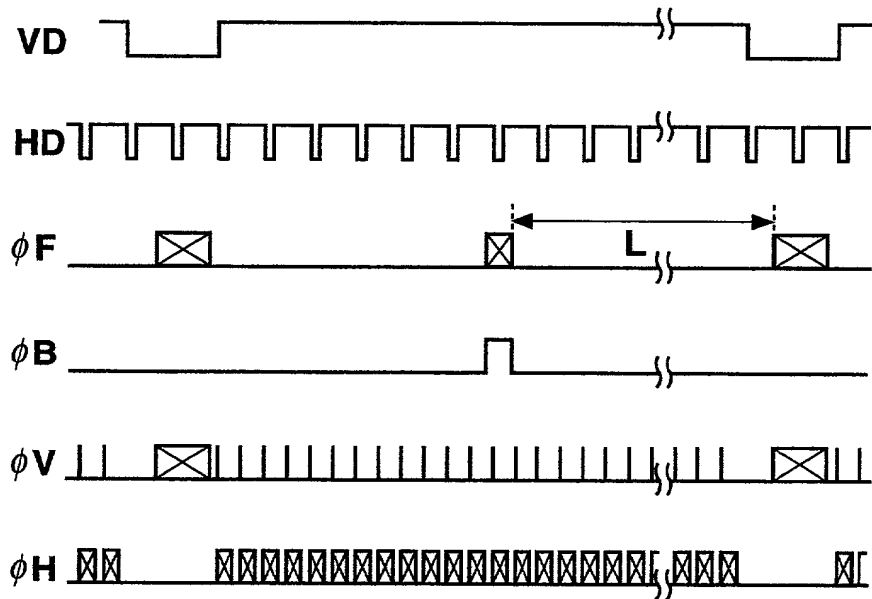


**Fig. 2 PRIOR ART**

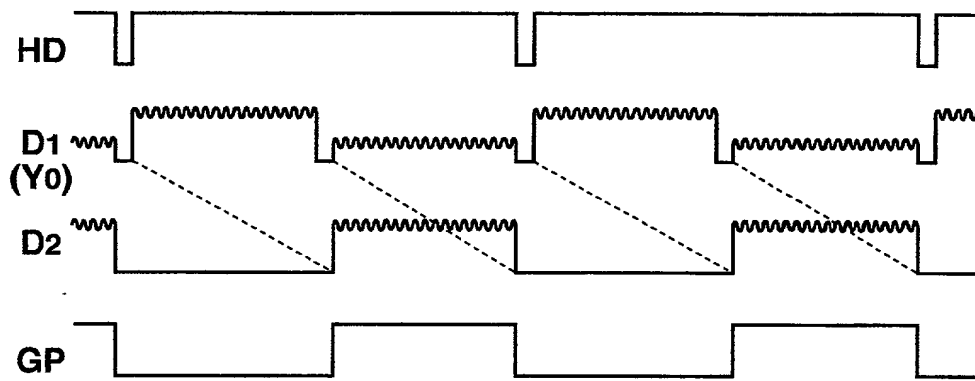




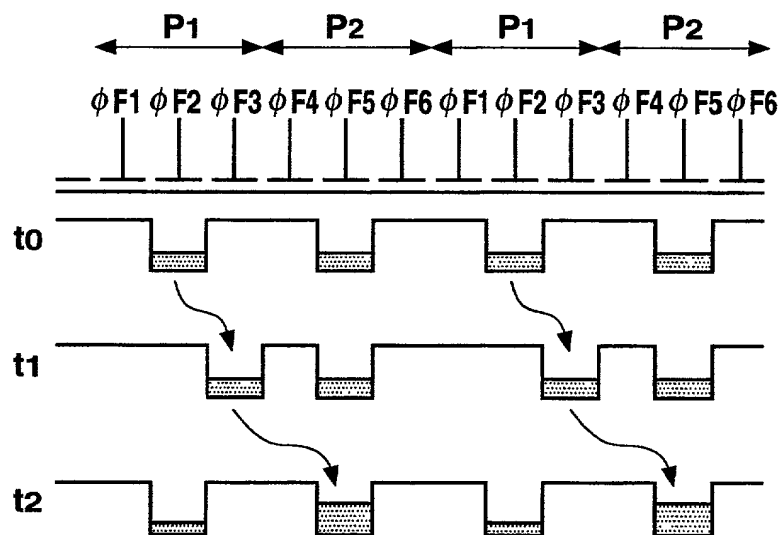
**Fig. 3**



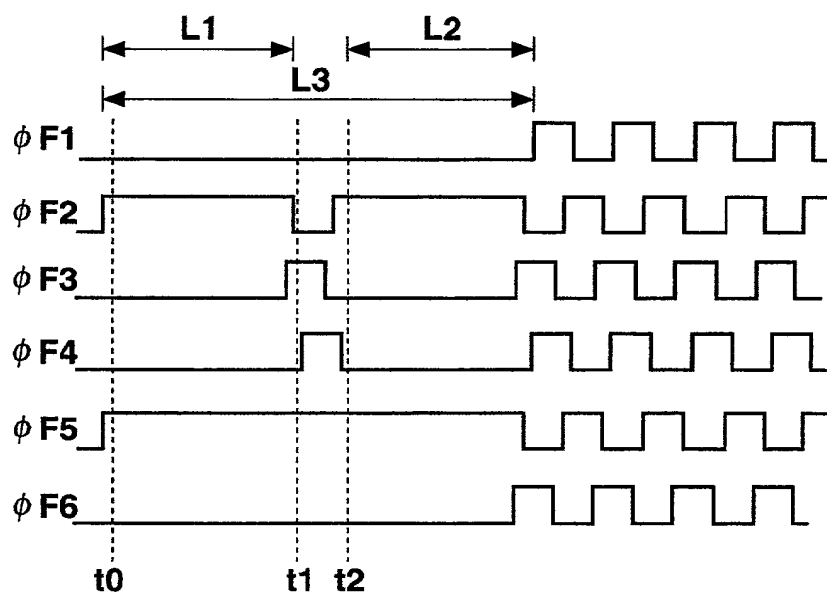
**Fig. 4**



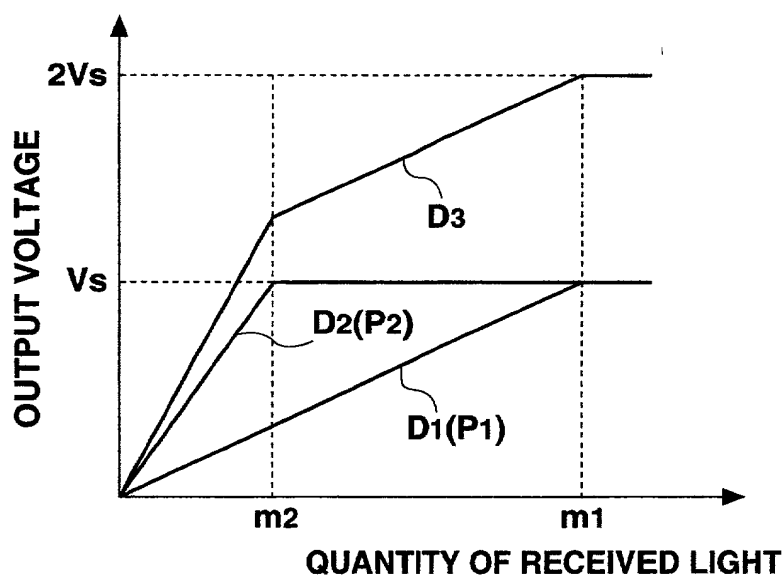
**Fig. 5**



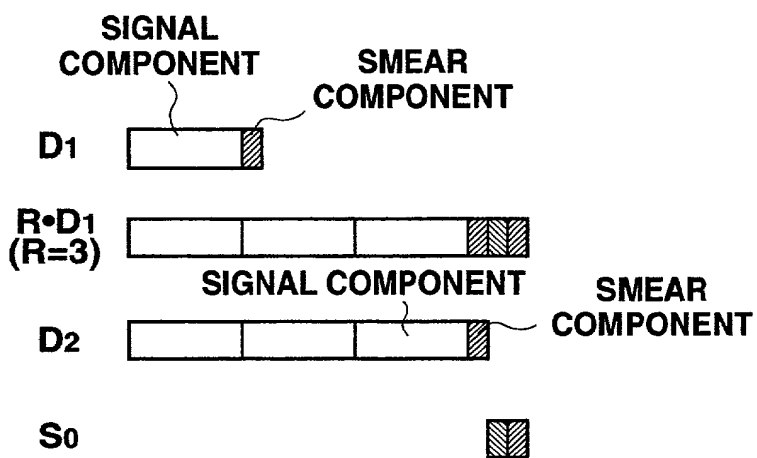
**Fig. 6**



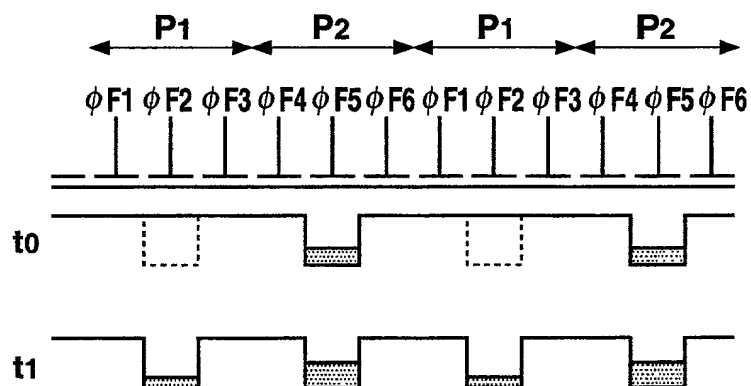
**Fig. 7**



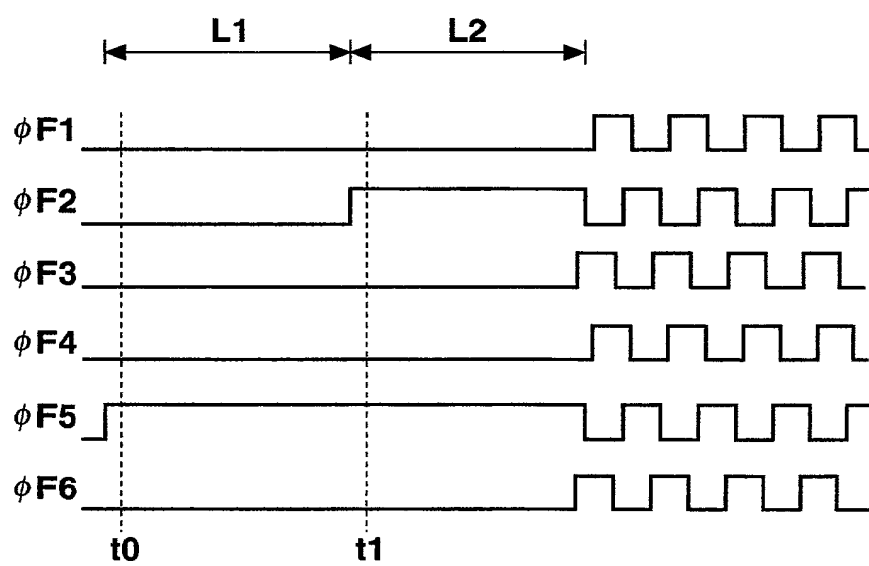
**Fig. 8**



**Fig. 9**



**Fig. 10**



**Fig. 11**

Attorney's Ref. No.: \_\_\_\_\_

## Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

## Japanese Language Declaration

## 日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は、下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SOLID-STATE IMAGE PICKUP APPARATUS

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ 年 月 日に提出され、米国出願番号または特許協定条約 国際出願番号を \_\_\_\_\_ とし、（該当する場合） \_\_\_\_\_ に訂正されました。☐ was filed on \_\_\_\_\_ as United States Application Number or PCT International Application Number \_\_\_\_\_ and was amended on \_\_\_\_\_ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

## Japanese Language Declaration

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私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基づき下記の、米国以外の国の少なくとも1ヶ国を指定している特許協力条約365条(a)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

## Prior Foreign Application(s)

外国での先行出願

Priority Not Claimed

優先権主張なし

Hei 11-73930

(Number)

(番号)

Japan

(Country)

(国名)

18/March/1999

(Day/Month/Year Filed)

(出願年月日)

(Number)

(番号)

(Country)

(国名)

(Day/Month/Year Filed)

(出願年月日)

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(Application No.)

(出願番号)

(Filing Date)

(出願日)

(Application No.)

(出願番号)

(Filing Date)

(出願日)

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(Application No.)

(出願番号)

(Filing Date)

(出願日)

(Status: Patented, Pending, Abandoned)

(現況: 特許許可済、係属中、放棄済)

(Application No.)

(出願番号)

(Filing Date)

(出願日)

(Status: Patented, Pending, Abandoned)

(現況: 特許許可済、係属中、放棄済)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

## Japanese Language Declaration

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委任状： 私は、下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。(弁護士、または代理人の氏名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

STUART LUBITZ, Reg. No. 20,680; LOUIS A. MOK, Reg. No. 22,585; JOHN P. SCHERLACHER, Reg. No. 23,009; MICHAEL J. RAM, Reg. No. 26,379; LEWIS ANTEN, Reg. No. 26,604; HIDEO KODA, Reg. No. 27,729; JoANNE S. REDMANN, Reg. No. 31,482; SONG K. JUNG, Reg. No. 35,210; WILLIAM H. WRIGHT, Reg. No. 36,312; JONATHAN Y. KANG, Reg. No. 38,199; DAVID L. LUBITZ, Reg. No. 38,229; WEI-NING YANG, Reg. No. 38,690; KARLTON BUTTS, Reg. No. 39,126

## 書類送付先:

LOEB & LOEB  
10100 Santa Monica  
Boulevard Suite 2200,  
Los Angeles, CA 90067-4164

## Send Correspondence to:

LOEB & LOEB  
10100 Santa Monica  
Boulevard Suite 2200,  
Los Angeles, CA 90067-4164

## 直接電話連絡先: (名前及び電話番号)

LOEB & LOEB  
301-282-2000

## Direct Telephone Calls to: (name and telephone number)

LOEB & LOEB  
301-282-2000

## 唯一または第一発明者名

## Full name of sole or first inventor

Tohru WATANABE

## 発明者の署名

日付

## Inventor's signature

Date

*Tohru Watanabe*

Feb. 29, 2000

## 住所

日本国

## Residence

Ogaki-shi, Gifu

Japan

## 国籍

日本

## Citizenship

Japan

## 私書箱

## Post Office Address

218-1, Aoyagi-cho 2-chome, Ogaki-shi, Gifu 503-0961, Japan

## 第二共同発明者

## Full name of second joint inventor, if any

## 第二共同発明者の署名

日付

## Second inventor's signature

Date

## 住所

日本国

## Residence

Japan

## 国籍

日本

## Citizenship

Japan

## 私書箱

## Post Office Address

(第三以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for third and subsequent joint inventors.)